19-1853; Rev 0; 11/00

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

General Description

The MAX3950 deserializer is ideal for converting 10Gbps serial data to 16-bit wide, 622Mbps parallel data in SDH/SONET and DWDM applications. Operating from a single +3.3V supply, this device accepts CML serial clock and data inputs, and delivers low-voltage differential-signal (LVDS) clock and data outputs for interfacing with high-speed digital circuitry.

The MAX3950 is available in the extended temperature range (-40°C to +85°C) in a 68-pin QFN package. The typical power dissipation is 900mW.

Applications

SONET/OC-192 SDH/STM-64 Transmission Systems

Add/Drop Multiplexers

Broadband Digital Cross-Connects

Features

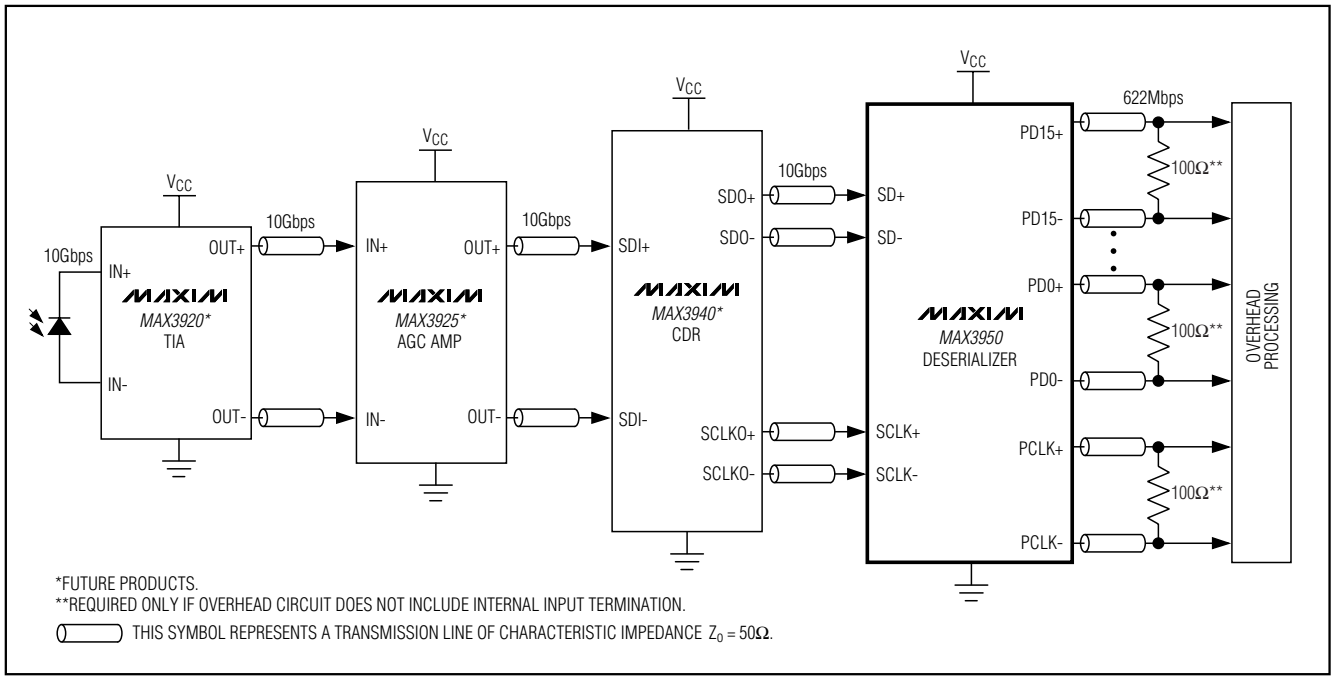
- ♦ **Supports Serial Data Rates Up to 10.7Gbps**
- ♦ **10Gbps/10.7Gbps Serial to 622Mbps/667Mbps Parallel Conversion**
- ♦ **Single +3.3V Supply**
- ♦ **900mW Operating Power**
- ♦ **CML Serial Clock and Data Inputs**
- ♦ **LVDS Parallel Clock and Data Outputs**
- ♦ **-40°C to +85°C Operating Temperature**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3950EGK	-40°C to +85°C	68 QFN

Pin Configuration appears at the end of data sheet.

Typical Application Circuit



+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC}).....-0.5V to +5.0V
CML Input Voltage Level.....(V_{CC} - 0.8V) to (V_{CC} + 0.5V)
LVDS Output Voltage Level.....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
68-Pin QFN (derate 43.5mW/°C above +85°C) 2800mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			270	350	mA
CML INPUTS (SD±, SCLK±)						
Differential Input Voltage Swing	V_{ID}		400		1200	mVp-p
Single-Ended Input Voltage Range	V_{IS}	Figure 1	V_{CC} - 0.6		V_{CC} + 0.3	V
Input Termination to V_{CC}	R_{IN}		42.5	50	57.5	Ω
LVDS OUTPUT SPECIFICATION (PD[15.0] ±, PCLK±)						
Output High Voltage	V_{OH}				1.375	V
Output Low Voltage	V_{OL}		1.025			V
Differential Output Voltage	$\|V_{OD}\|$	Figure 2	150		250	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\|V_{OD}\|$				25	mV
Offset Output Voltage			1.15		1.25	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$				25	mV
Differential Output Impedance			80		120	Ω
Output Current		Short together			12	mA
		Short to ground			24	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω ±1%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Input Data Rate				10		Gbps
Serial Data Setup Time	t_{SU}		25			ps
Serial Data Hold Time	t_H		25			ps
Parallel Output Data Rate				622		Mbps
Parallel Output Clock Frequency				622		MHz
Parallel Clock to Q Delay	t_{CLK-Q}	(Note 2)	-200		200	ps
LVDS Output Rise/Fall Time		(20% to 80%)			300	ps
LVDS Differential Skew	t_{SKEW1}	Any differential pair			65	ps
LVDS Channel-to-Channel Skew	t_{SKEW2}	PD[15..0]±		200		ps
Input Return Loss	$\|S_{11}\|$	100kHz ≤ f ≤ 5GHz		17		dB
		5GHz ≤ f ≤ 10GHz		14		
		10GHz ≤ f ≤ 15GHz		11		

Note 1: AC specifications are guaranteed by design and characterization.
Note 2: Relative to the falling edge of PCLK+. See Figure 3.

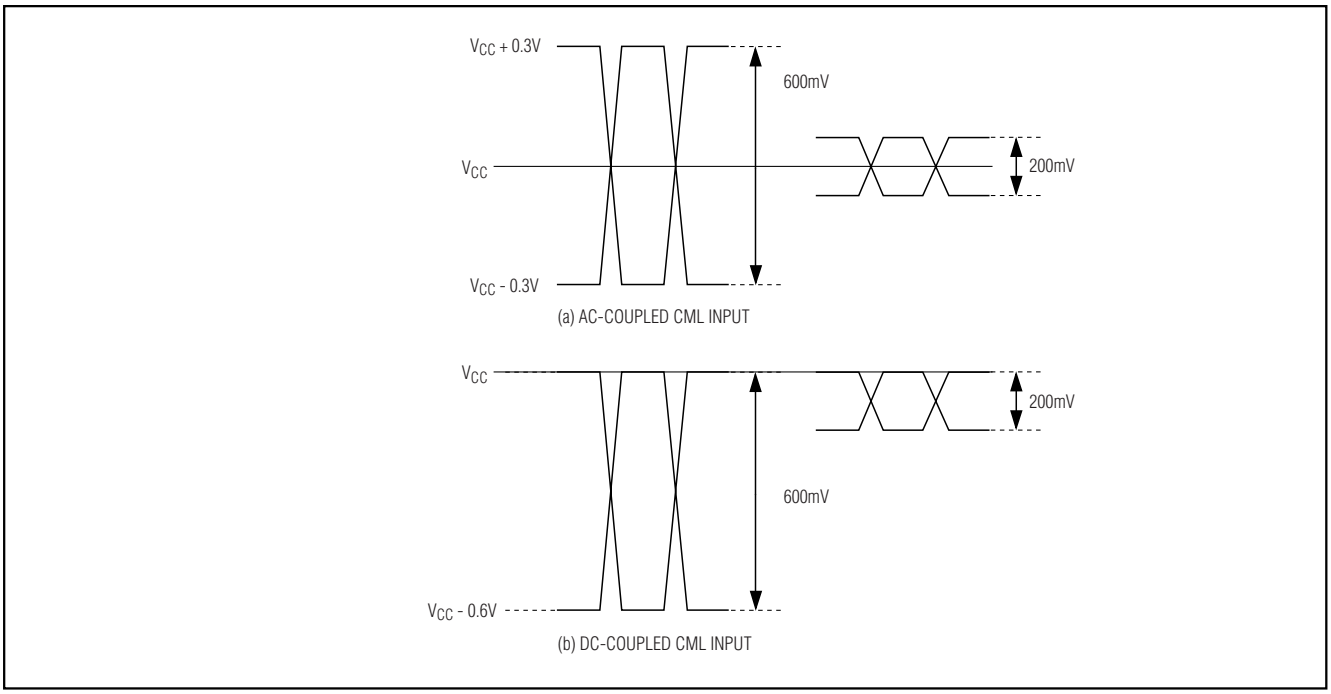


Figure 1. Input Amplitude

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

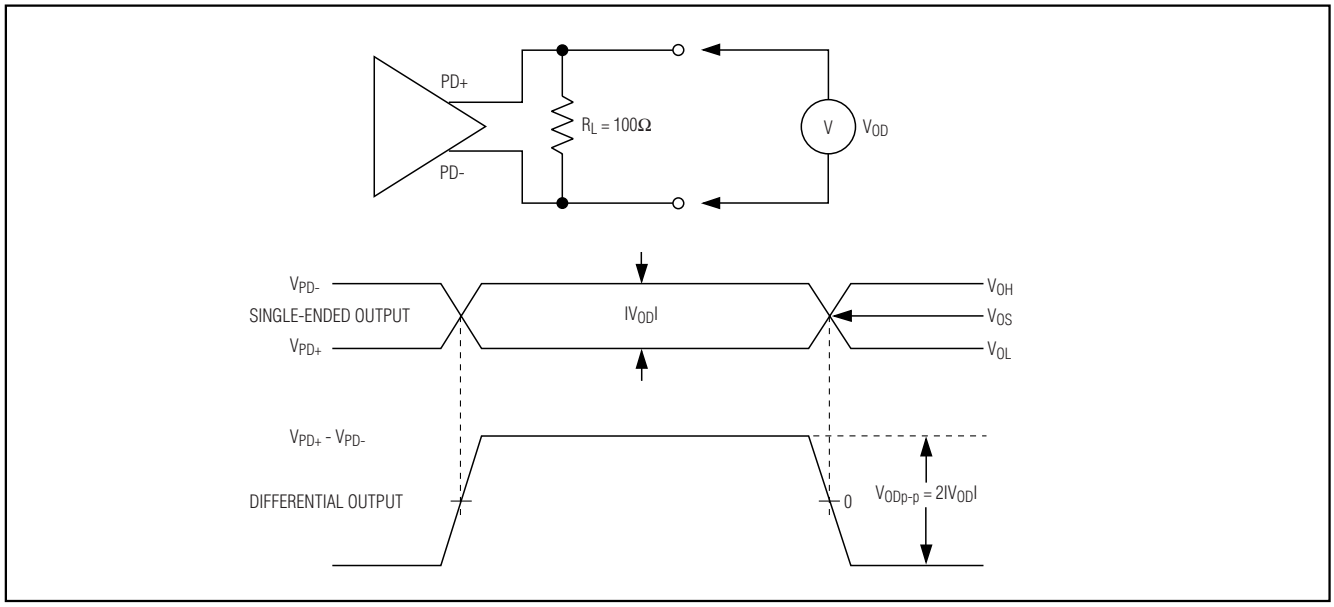


Figure 2. Driver Output Levels

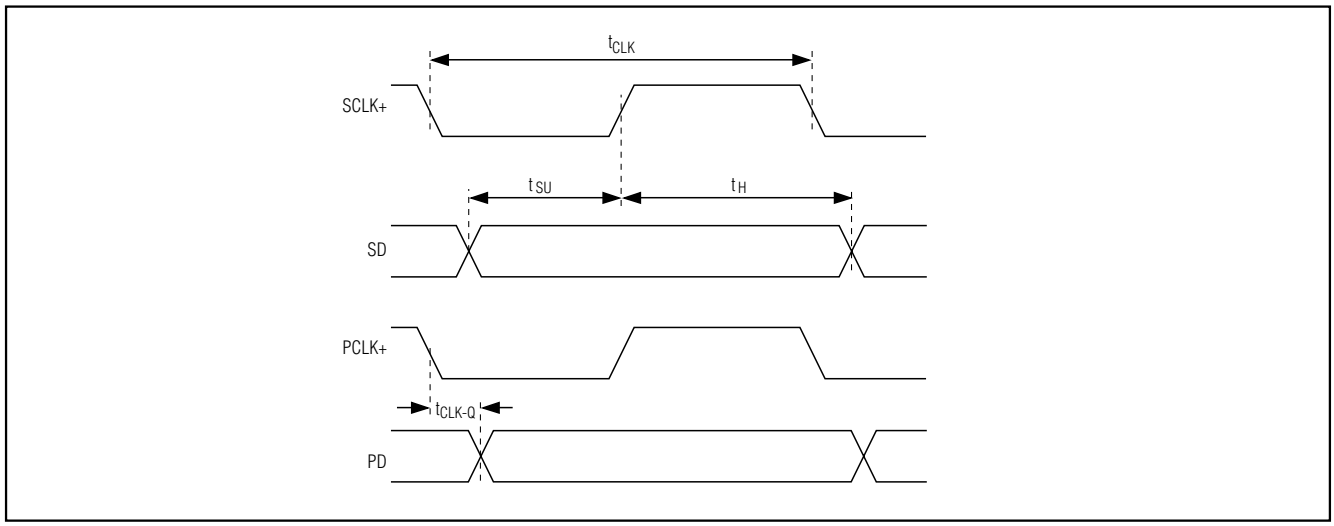


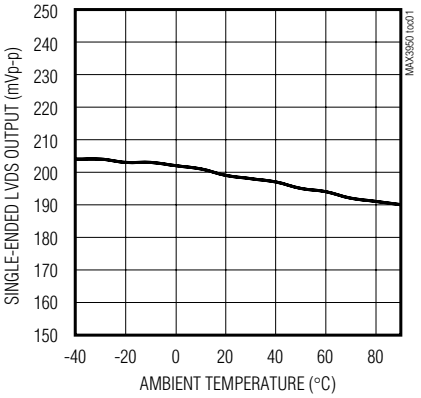
Figure 3. Timing Parameters

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

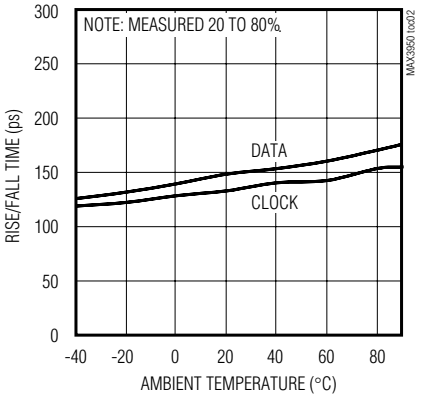
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

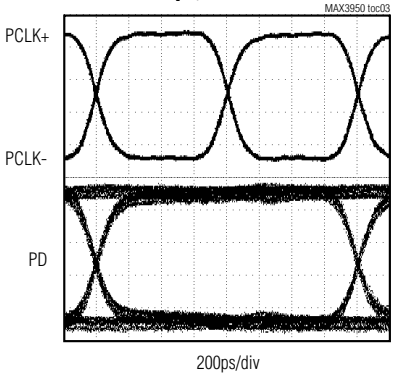
LVDS OUTPUT AMPLITUDE vs. TEMPERATURE



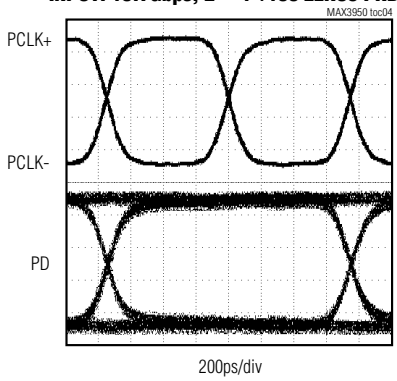
OUTPUT RISE/FALL TIME vs. TEMPERATURE



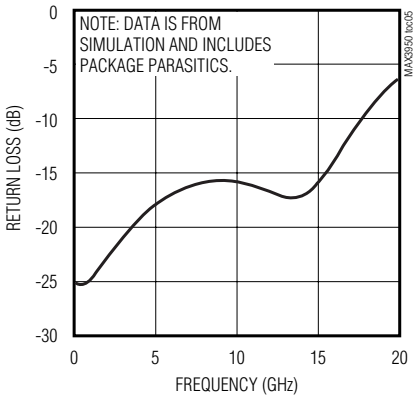
OUTPUT EYE DIAGRAM INPUT: 9.953Gbps, 2^{13} -1 +100 ZEROS PRBS



OUTPUT EYE DIAGRAM INPUT: 10.7Gbps, 2^{13} -1 +100 ZEROS PRBS



INPUT RETURN LOSS



Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 13, 16, 17, 18, 26, 33–36, 42, 51, 52, 53, 60, 68	GND	Ground
6, 9, 12, 25, 31, 32, 37, 43, 50, 54, 55, 61	V_{CC}	Positive Power Supply
7	SD+	Positive Data Input. 9.953Gbps serial data stream, CML.
8	SD-	Negative Data Input. 9.953Gbps serial data stream, CML.
10	SCLK+	Positive Serial Clock Input. 9.953GHz, CML.
11	SCLK-	Negative Serial Clock Input. 9.953GHz, CML.
14	PCLK-	Negative Parallel Clock Output, 622.08MHz, LVDS.

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

Pin Description (continued)

PIN	NAME	FUNCTION
15	PCLK+	Positive Parallel Clock Output, 622.08MHz, LVDS.
19, 21, 23, 27, 29, 38, 40, 44, 46, 48, 56, 58, 62, 64, 66, 3	PD0- to PD15-	Negative Parallel Data Output, 622.08Mbps, LVDS.
20, 22, 24, 28, 30, 39, 41, 45, 47, 49, 57, 59, 63, 65, 67, 4	PD0+ to PD15+	Positive Parallel Data Output, 622.08Mbps, LVDS.
EP	Exposed Pad	Ground. This must be soldered to the circuit board ground for proper thermal and electrical operation. See *Layout Considerations.*
CP	Corner Pins	Ground. The corner pins are connected to the exposed pad through the lead frame. If the corner pins are not soldered to the same node as the exposed pad, ensure that the solder mask is located below them so that unintentional connections do not occur.

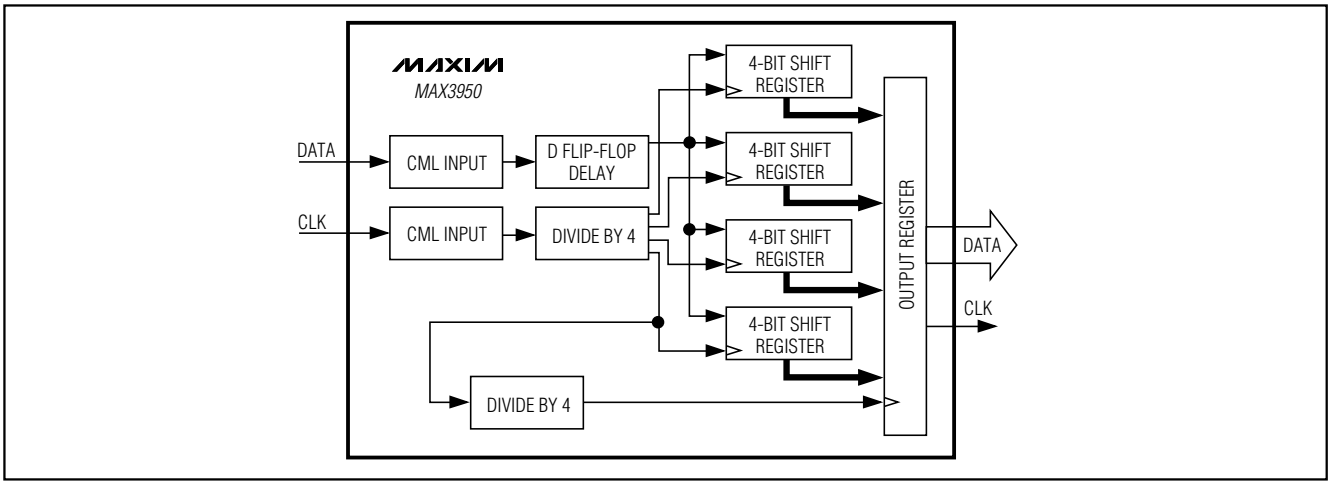


Figure 4. Functional Block Diagram

Detailed Description

The MAX3950 deserializer implements a shift-register-based demultiplexer to convert 9.953Gbps serial data to 16-bit wide, 622.08Mbps parallel data (Figure 4). The allocation of the serial input bits to the parallel LVDS outputs is displayed in Figure 5.

Applications Information

Low-Voltage Differential-Signal Outputs

The MAX3950 features LVDS outputs for interfacing with high-speed digital circuitry. This LVDS implementation is based on the IEEE 1596.3 LVDS reduced-range link specification and is compatible with OIF 1999.102. Note that the PCLK polarity on the MAX3950 is inverted relative to OIF 1999.102, so that PCLK+ is equivalent to RXCLK_N and PCLK- is equivalent to RXCLK_P.

The MAX3950 uses 300mVp-p to 500mVp-p differential low-voltage swings to achieve fast transition times, minimize power dissipation, and improve noise immunity. The parallel clock and data LVDS outputs (PCLK+, PCLK-, PD_+, PD_-) require 100Ω differential DC termination between the inverting and noninverting outputs for proper operation. Do not terminate these outputs to ground. For more information on interfacing with the

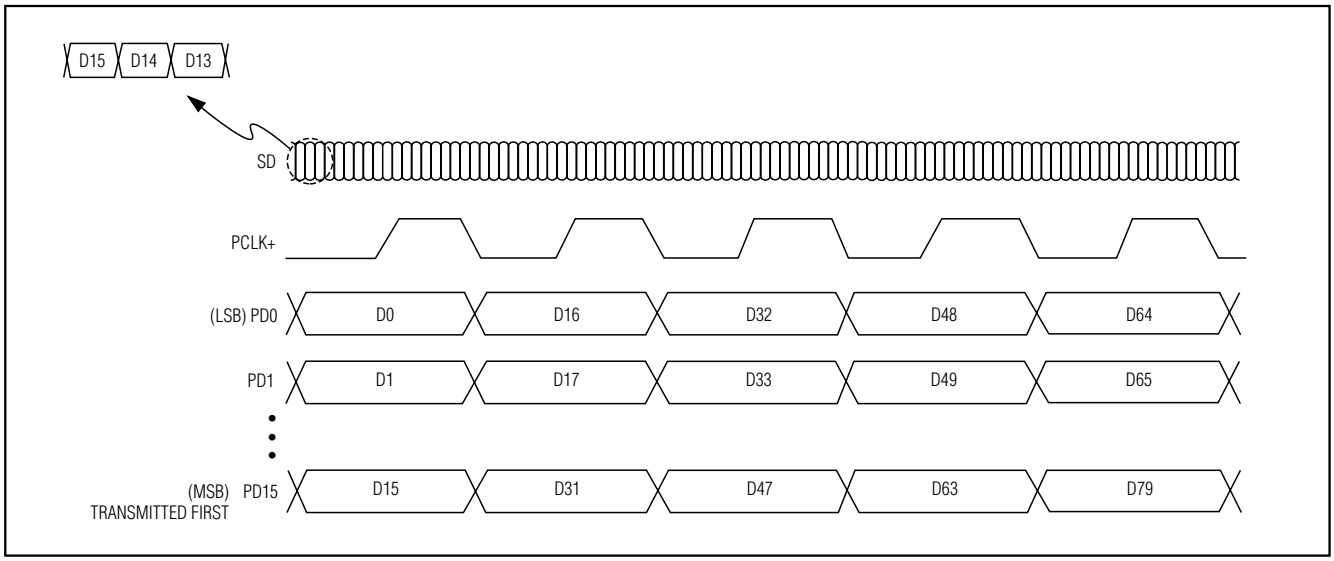


Figure 5. Timing Diagram

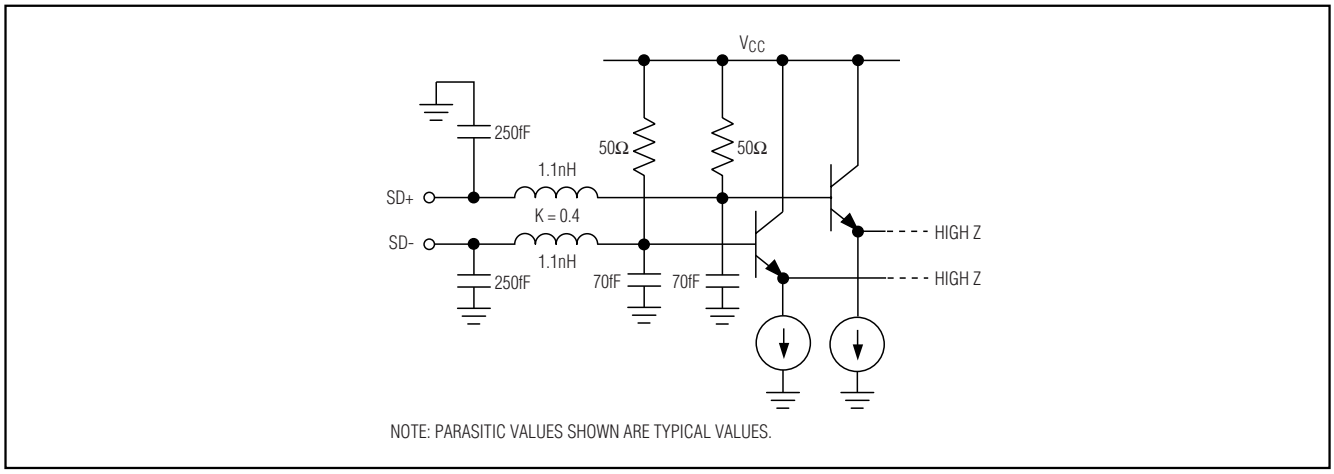


Figure 6. CML Input Model

LVDS outputs, refer to Maxim Application Note *HFAN-1.0 Interfacing Between CML, PECL, and LVDS*.

Current Mode Logic (CML) Inputs

The differential serial inputs to the MAX3950 are CML and have an input impedance of 50Ω on each of the complementary inputs. For more information on interfacing with the CML inputs, refer to Maxim Application Note *HFAN-1.0 Interfacing Between CML, PECL, and LVDS*.

Interface Models

Figures 6 and 7 show the typical input/output models for the MAX3950 deserializer.

Layout Considerations

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3950's high-speed inputs and outputs. Power-supply decoupling should be placed as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

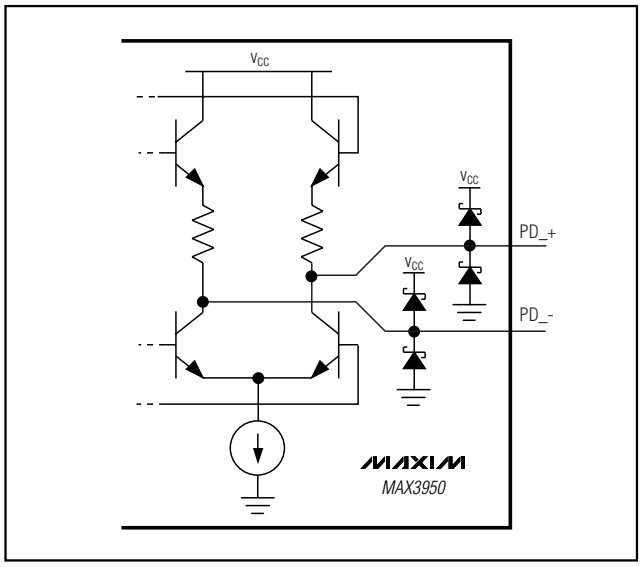


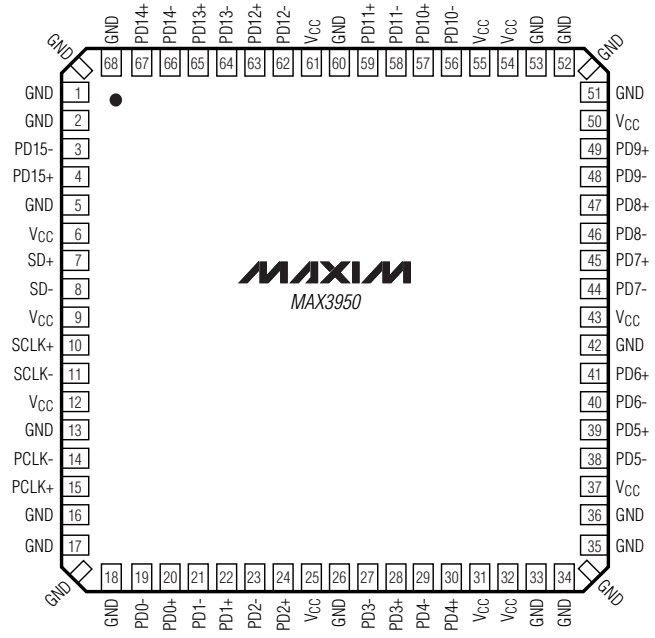
Figure 7. LVDS Output Model

Chip Information

TRANSISTOR COUNT: 4800

Pin Configuration

TOP VIEW

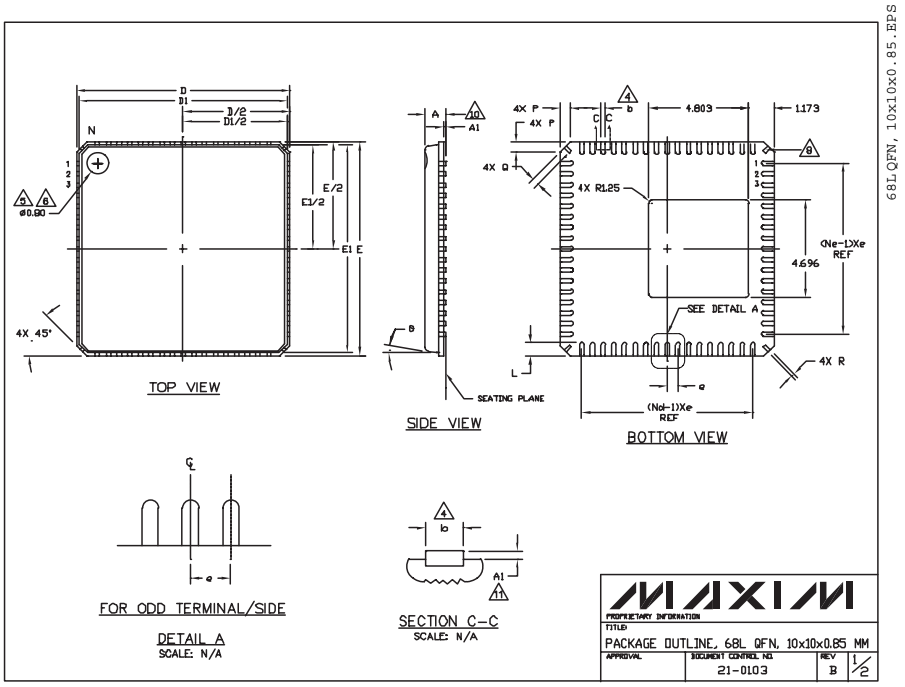


QFN*

*EXPOSED PAD IS CONNECTED TO GND.

+3.3V, 10.7Gbps 1:16 Deserializer with LVDS Outputs

Package Information



NOTES:

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TERMINAL.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPES SHOWN AT FOUR CORNERS ARE CONNECTED TO DIE PAD.
9. PACKAGE WARPAGE MAX 0.10mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
11. APPLIED ONLY FOR TERMINALS.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00BSC		
D1		9.75BSC		
E		10.00BSC		
E1		9.75BSC		
N		68		3
Nd		17		3
Ne		17		3
e		0.50 BSC		
L	0.50	0.60	0.75	
θ			12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	
R	0.13	0.17	0.23	